

Notice of References Cited	Application/Control No. 10/630,800		Applicant(s)/Patent Under Reexamination IMADE ET AL.	
	Examiner Belur V Keshavan		Art Unit 2825	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
X	A	US-2003/0107103	06-2003	Iwata et al.	257/506
X	B	US-2002/0105034	08-2002	Iwata et al.	257/368
X	C	US-5,994,756	11-1999	Umezawa et al.	257/510
X	D	US-5,275,965	01-1994	Manning, Monte	438/430
X	E	US-5,897,361	04-1999	Egawa, Hidemitsu	438/435
X	F	US-6,281,081	08-2001	Chien et al.	438/296
X	G	US-5,256,591	10-1993	Jun, Young K.	438/424
X	H	US-6,436,790	08-2002	Ito, Shinya	438/424
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	05-304205	11-1993	JP	Kiotoshi	H01L 21/76
	O	11-176924	07-1999	JP	Ri-Kanshin	H01L 21/76
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	G. Scott et al., NMOS Drive Current Reduction Caused By Transistor Layout And Trench Isolation Induced Stress, IEDM 99-827, pp 34.4.1-34.4.4, 1999 IEEE.
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.